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EXAMINER

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2827

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Please find below and/or attached an Office communication concerning this application or proceeding.

## 2827

Part of Paper No. 12

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to because Figures are improperly crosshatched. All of the parts shown in the section, and only those parts, must be crosshatched. The crosshatching patterns should be selected from those shown on page 600-81 of the MPEP based on the material of the part. See also 37 CFR 1.84(h)(3) and MPEP 608.02. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.
2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "at least one clearance between said electrically conductive circuitry and said plated through hole" must be shown or the feature(s) canceled from the claim(s). In the drawings the clearance is between the power plane and the through hole. In addition, the limitation that the plated through hole is electrically coupled to an electrically conductive circuitry, is not shown in the drawings. No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 8,13, and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claim 8, it is not clear from the specification or the drawings, how can the clearance be located between the electrically conductive circuitry and the plated through hole, if the plated through hole is electrically coupled to the electrically conductive circuitry. It is further unclear, which one of the clearance or the through hole, is filled with said dielectric material. In the case that it is the through hole that is filled with said dielectric material, it might raise 112 1<sup>st</sup> paragraph issues. In addition, Claim 8 recites the limitation "said plated through hole filled with said dielectric material" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Regarding Claim 13, the recitation: "said power plane is spaced from said through hole" is not clear. Is it that the plated through hole goes through the power plane or if the plated through hole is separated from the power plane. In addition, the claim recites the limitation "the space between said power plane and said through hole" in line 4. There is insufficient antecedent basis for this limitation in the claim. In addition, it is unclear if the "non-conductive layer" of line 3, is a different "non-conductive layer" than the one recited in claim 48, or if it is the same layer.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3,6,8 rejected under 35 U.S.C. 102(b) as being anticipated by Tsukada et al. (US Patent NO. 5,451,721).

Regarding Claim 1, Tsukada teaches a printed circuit board comprising: a substrate layer (Reference number 10) comprising impregnated glass fibers; a non-conductive layer (combination of Reference numbers 18,22,28) comprising a dielectric material free of continuous glass fibers (Reference number 18); and an electrically conductive circuitry (Reference number 44) comprising a conductive material formed on said non-conductive layer such that said non-conductive layer lies between said substrate layer and said conductive material.

The recitations: "for use in an electronic device package" and "to prevent shorts there between caused by migration of said conductive material along said glass fibers" are intended use limitations, and it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex Parte Masham*, 2 USPQ F.2d 1647 (1987).



Regarding Claim 2, Tsukada teaches a plated through hole (Reference number 38) extending through said substrate layer and said non-conductive layer and electrically coupled to said circuitry.

Regarding Claim 3, Tsukada teaches that the dielectric material comprises a photoimageable dielectric material (column 2, lines 66-68).

Regarding Claim 6, Tsukada teaches that the dielectric material is a resin (Reference number 18) coating a copper foil (Reference number 16).

Regarding Claim 8, as best understood by the examiner Tsukada teaches at least one clearance (the space between reference numbers 40 and 38) between said electrically conductive circuitry and said plated through hole filled with said dielectric material.

7. Claims 48,10,12-15,19,22 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsukada et al. (US Patent NO. 5,451,721).

Regarding Claim 48, Tsukada teaches an electronic device package (device of Figure 2I) comprising: a substrate (Reference number 10) comprising impregnated glass fibers; an electrically conductive circuit (Reference numbers 40,42); and a non-conductive layer (combination of Reference numbers 18,22,28) comprising a dielectric material free of continuous glass fibers (Reference number 18) applied to said substrate such that said non-conductive layer lies between said substrate and said electrically conductive circuit (See Figure 2I).

The recitation: "to prevent shorts there between caused by migration of said electrically conductive circuit along said glass fibers" is an intended use limitation, and it

has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987).

Regarding Claim 10, Tsukada teaches at least one power plane (Reference number 44).

Regarding Claim 12, Tsukada teaches at least one plated through hole (Reference number 38) extending through said substrate and said non-conductive layer.

Regarding Claim 13, as best understood by the examiner Tsukada teaches that said power plane (Reference number 44) is spaced from said through hole (See figure 38) and said board includes a non-conductive layer comprising a dielectric material free of continuous glass fibers in the space between said power plane and said through hole. The recitation "to prevent a short there between" is merely an intended use of the non-conductive layer, and it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987).

Regarding Claim 14, Tsukada teaches that the non-conductive layer is positioned between said through hole and said electrically conductive circuit (See figure 21).

Regarding Claim 15, Tsukada teaches at least one clearance (the space between reference numbers 40 and 38) filled with said dielectric material (See Figure 21)

Regarding Claims 19, Tsukada teaches that the dielectric material comprises a photoimageable dielectric material (olumn 2, lines 66-68).

Regarding Claim 22, Tsukada teaches that the dielectric material comprises resin-coated copper foil (Reference number 18, coating Reference number 16).

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 4,5 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukada et al. (US Patent No. 5,451,721).

Regarding Claims 4 and 5, Tsukada teaches all the limitations of the instant claimed invention as stated supra for claim 1, but fails to explicitly teach that the dielectric material comprises a polyimide, or a Kevlar-based paper impregnated with epoxy resin. The use of a polyimide and Kevlar-based paper impregnated with epoxy resin, as dielectric material of a printed circuit board is well known in the art. Both materials are well used in the art for their excellent dielectric properties. It would have been obvious to one of ordinary skill in the art at the time of the invention, to use any of these two materials as the material of the dielectric, to achieve the desired dielectric characteristic for the printed circuit board. In addition it has been held to be within the



Art Unit: 2827

general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding Claim 37, Tsukada teaches all the limitations of the instant claimed invention as stated supra for claim 1, but fails to explicitly teach that the thickness of said non-conductive layer is between 0.5 mils and 5 mils. It is well known in the art to make the layers of a printed circuit board as small as possible, to improve integration. It would have been obvious to one of ordinary skill in the art at the time the invention was made to reduce the thickness of the non-conductive layer in order to improve integration. In addition it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. See In re Aller, 105 USPQ 233.

10. Claims 20,21 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukada et al. (US Patent No. 5,451,721).

Regarding Claims 20 and 21, Tsukada teaches all the limitations of the instant claimed invention as stated supra for claim 48, but fails to explicitly teach that the dielectric material comprises a polyimide, or a Kevlar-based paper impregnated with epoxy resin. The use of a polyimide and Kevlar-based paper impregnated with epoxy resin, as dielectric material of a printed circuit board is well known in the art. Both materials are well used in the art for their excellent dielectric properties. It would have been obvious to one of ordinary skill in the art at the time of the invention, to use any of these two materials as the material of the dielectric, to achieve the desired dielectric characteristic for the printed circuit board. In addition it has been held to be within the

Art Unit: 2827

general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding Claim 38, Tsukada teaches all the limitations of the instant claimed invention as stated supra for claim 48, but fails to explicitly teach that the thickness of said non-conductive layer is between 0.5 mils and 5 mils. It is well known in the art to make the layers of a printed circuit board as small as possible, to improve integration. It would have been obvious to one of ordinary skill in the art at the time the invention was made to reduce the thickness of the non-conductive layer in order to improve integration. In addition it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. See In re Aller, 105 USPQ 233.

11. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukada et al. (US Patent No. 5,451,721) in view of Pellegrino (US Patent No. 4,521,262).

Regarding Claim 7, Tsukada teaches all the limitations of the instant claimed invention as stated supra for claim 1, but fails to explicitly teach that said substrate layer is prepreg comprising a glass fabric impregnated with epoxy resin. Pellegrino teaches a substrate layer that is prepreg comprising a glass fabric impregnated with epoxy resin (Column 4, lines 60-63). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Tsukada and Pellegrino in order to have a substrate layer that is prepreg comprising a glass fabric impregnated with epoxy resin, thus making it easy and fast to mass produce the substrate ready for component connections.

12. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukada et al. (US Patent No. 5,451,721) in view of Pellegrino (US Patent No. 4,521,262).

Regarding Claim 7, Tsukada teaches all the limitations of the instant claimed invention as stated supra for claim 48, but fails to explicitly teach that said substrate layer is prepreg comprising a glass fabric impregnated with epoxy resin. Pellegrino teaches a substrate layer that is prepreg comprising a glass fabric impregnated with epoxy resin (Column 4, lines 60-63). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Tsukada and Pellegrino in order to have a substrate layer that is prepreg comprising a glass fabric impregnated with epoxy resin, thus making it easy and fast to mass produce the substrate ready for component connections.

### ***Response to Arguments***

13. Applicant's arguments with respect to claims 1-8,10,12-15,19-23,37,38 and 48 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references teach some of the elements of the instant claimed invention: Ors et al. (US Patent No. 4,511,757), Sasaki et al. (US Patent No. 5,994,771), Inagaki et al. (US Patent No. 5,837,155), Uno et al. (US Patent No.

Application/Control Number: 09/342,584  
Art Unit: 2827

Page 11

5,827,604), Lando et al. (US Patent No. 4,888,450), Zweben et al. (US Patent No. 4,888,247), Pellegrino (US Patent No. 4,631,100), Murata (US Patent No. 6,400,010).

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jose H Alcala whose telephone number is (703) 305-9844. The examiner can normally be reached on Monday to Friday.

16. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JHA  
December 13, 2002

  
ALBERT W. PALADINI  
PRIMARY EXAMINER